Fraunhofer IPMS

Low Latency Ethernet Media Access Controller

LLEMAC-1G

The LLEMAC-1G is an Ethernet media access controller core that is compatible with the 10/100/1000 Mbps IEEE 802.3 and 1 Gbps IEEE 802.3-2002 specifications. The core offers extremely low input and output latency, making it ideal for implementation in Ethernet TSN nodes and other devices that require very low latency when receiving and sending Ethernet frames.

LLEMAC-1G is ready for functional safe system development according to ISO 26262 “Road vehicles – Functional safety”. ISO 26262 defines automotive safety integrity levels (ASIL) and LLEMAC-1G has been certified as “ASIL D ready” by the world’s leading testing, inspection and certification company SGS TÜV Saar GmbH. Therefore a safety enhanced version of the core is available, which implements clock activity monitors and utilizes spatial redundancy. DMR (dual mode redundancy) and DMR-LS (lockstep) are configurable. To ease the safety certification of systems using LLEMAC-1G FMEDA and SAM are shiped with the safety package.

The core is provided in Verilog RTL or as a targeted FPGA netlist and contains everything needed for a successful implementation, including a test bench, sample scripts, and extensive documentation.

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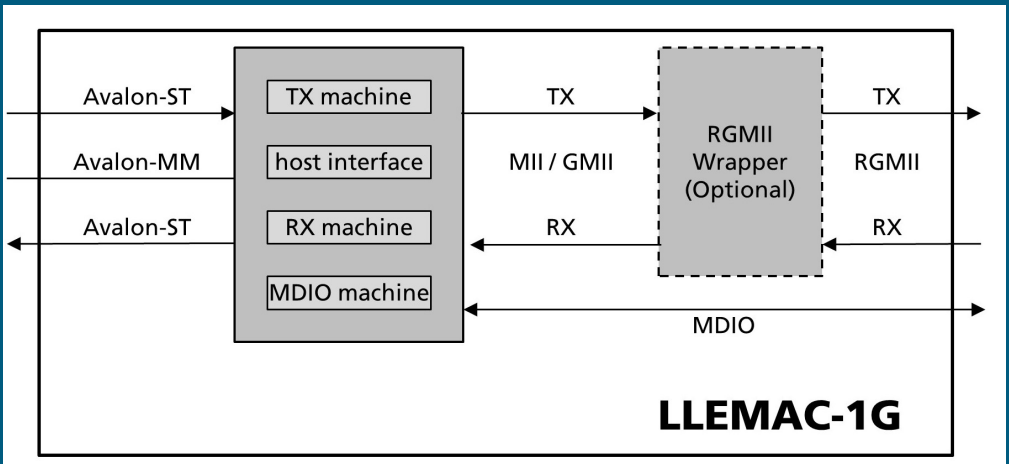


Features

- Triple Speed 10/100/1000 Mbps Low Latency Ethernet MAC
- Supports 10BASE-T1S, 10BASE-T, 100BASE-T and 1000BASE-T operation
- Supports IEEE 802.3
- Enables high-precision synchronization in TSN networks
- Egress latency: 10 Tx clock cycles
- Ingress latency: 6 Rx clock cycles
- Full duplex /Half Duplex point-to-point links

Interfaces

- Media Independent Interface (MII) for 10/100 Mbps
- Gigabit Media Independent Interface (GMII) for 1Gbps
- Reduced Gigabit Media Independent Interface (RGMII) for 10/100/1000 Mbps
- Serial Gigabit Media Independent Interfac (SGMII) for FPGA (for ASIC on request)
- MDIO interface for PHY configuration and management
- Host Interfaces to AXI, Avalon-ST/MM

Easy System Integration

- Platform independent implementation Xilinx, Intel, Microsemi, Lattice, Gowin FPGAs and any foundry technology
- Silicon proven
- Autonomous operation, requires no host assistance once programmed
- Responsive implementation support

Deliverables

- Source code Verilog RTL or targeted netlist
- Testbench
- Sample synthesis and simulation scripts
- Comprehensive documentation

Safety Enhanced Package

- SAM and FDMEA certified ISO-26262 ASIL D ready
- Spatial redundancy for inner logic protection
- ISO-26262 documentation package
- Clock activity monitoring

MACsec IP Core controller

Fraunhofer IPMS offers a MACSec IP Core Controller which is used for authentication and encryption of data packets between ethernet network devices. It can be used with the LLEMAC core or in standalone operations.

Fraunhofer IPMS

MAC-SEC

MACsec Controller IP Core

Media Access Control Security

The MACsec Controller IP Core MAC-SEC for data rates up to 10G implements the Layer 2 security standard specified in IEEE 802.1AE-2018, which provides authentication, confidentiality, and integrity between hosts in a Local Area Network (LAN). MACsec ensures that only authorized nodes on the LAN are allowed to communicate, provides confidentiality by encrypting transmitted data, and provides cryptographic mechanisms that ensure data integrity. It can be used with the Fraunhofer IPMS LLEMAC IP core, any other Ethernet MAC IP core or in standalone operations.

Features

- Fully synchronous and synthesizable HDL design (System Verilog)
- Supports MACsec specification (IEEE 802.1AE-2018) and IEEE Std802.1AEbw
  - GCM-AES-128/192/256
  - GCM-AES-XPN-128/192/256
- Supports NIST encryption Standards
  - Advanced Encryption Standard (AES) FIPS PUB 197
  - Galois Counter Mode (GCM) RFC 5647
  - Key size of 128, 192, or 256 bits
  - Verified with Galois/Counter Mode (GCM) and GMAC Validation System (GCMVS)
- Supports up to 2^16 (per synthesis parameter) secure associations
- Detailed error reporting

MAC Data Interface

- AXI stream interface for MAC data
  - Full duplex usage possible

Host Controller Interfaces

- 32 bit synchronous host controller interface; wrapper for 8 bit hosts
- 32 bit AMBA APB Protocol Specification v2.0
- 32 bit AMBA 3 AHB-Lite Protocol v1.0
- 32 bit Avalon-MM version 2018.09.26, simple interface (no pipelining)
- 32 bit Wishbone
- Optional application specific interface to the host-controller on request

Deliverables

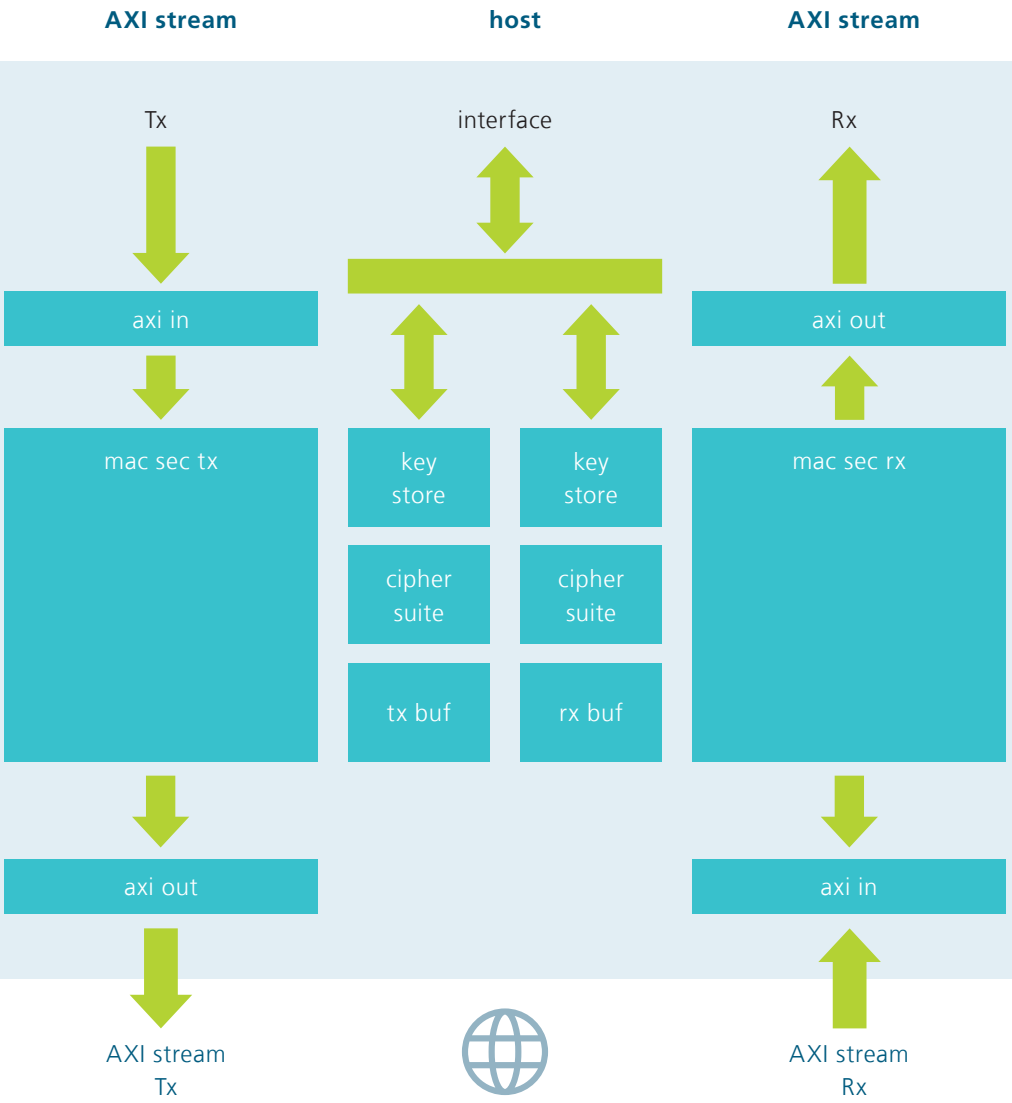
- Source code system Verilog RTL or targeted netlist
- Testbench
- Sample synthesis and simulation scripts
- Comprehensive documentation

Easy System Integration

- Platform independent implementation into any FPGA and any foundry technology
- Responsive implementation support

Low Latency Ethernet MAC Controller Core

Fraunhofer IPMS offers an IP core that implements an Low Latency Ethernet Media Access Controller (LLEMAC) that is compatible with the IEEE 802.3 and IEEE 802.3- 2002 specifications at 10/100 Mbps and 1Gbps. It has extremely low input and output latency. It is certified as ASIL-D-ready according to ISO 26262 for functional safety.



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